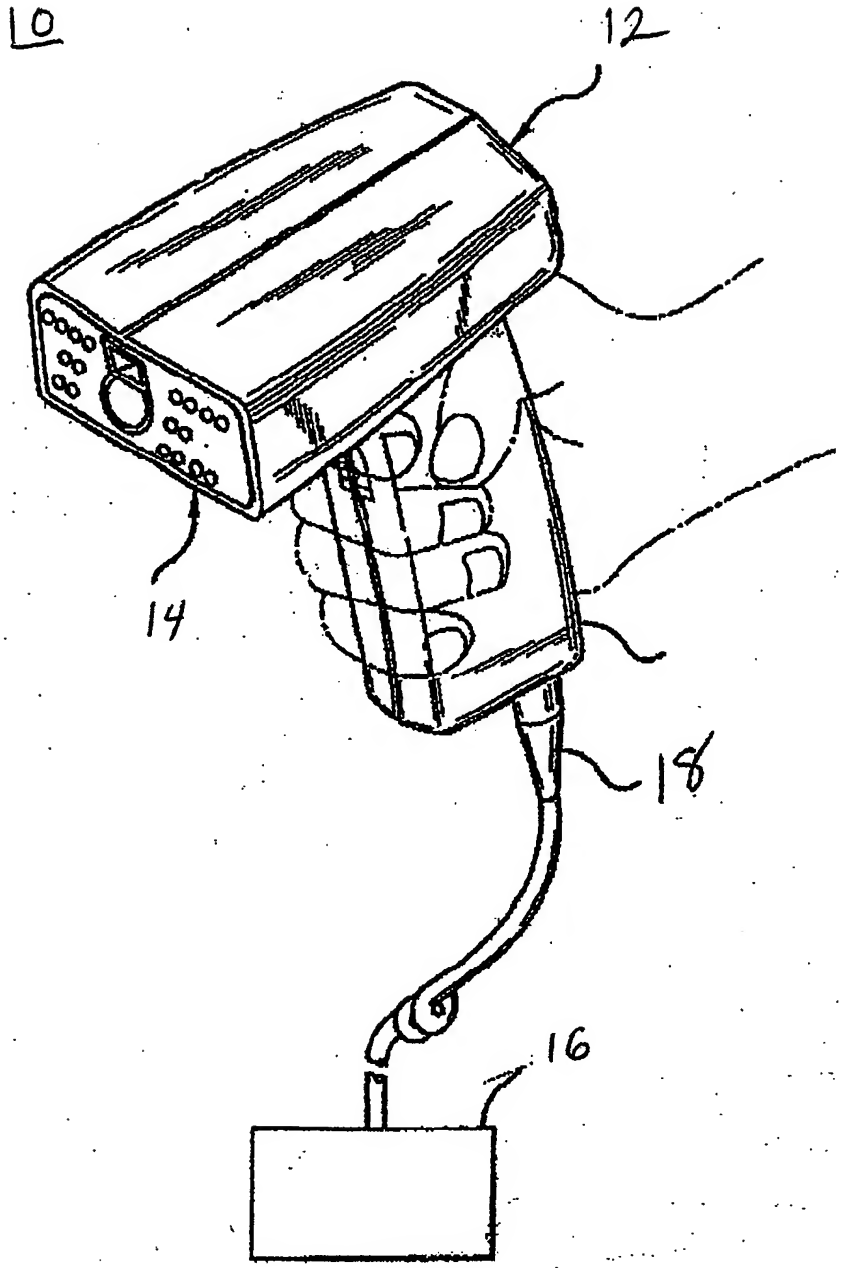


FIG. 1

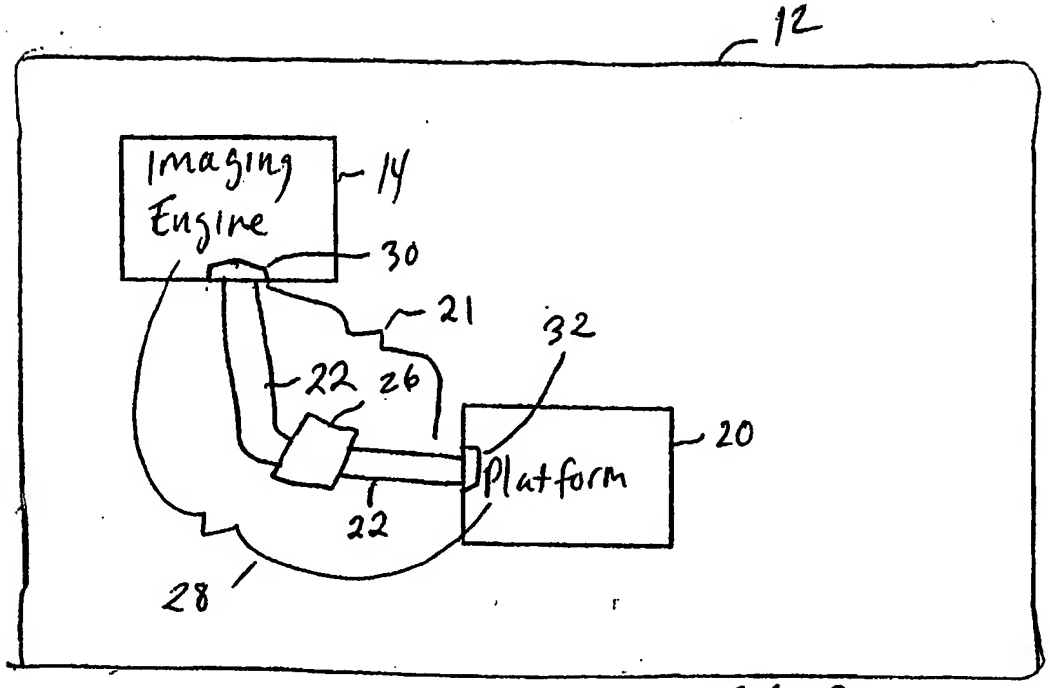
12
Imaging Engine
14
30
21
32
22
26
20
Platform
22
28

FIG. 2

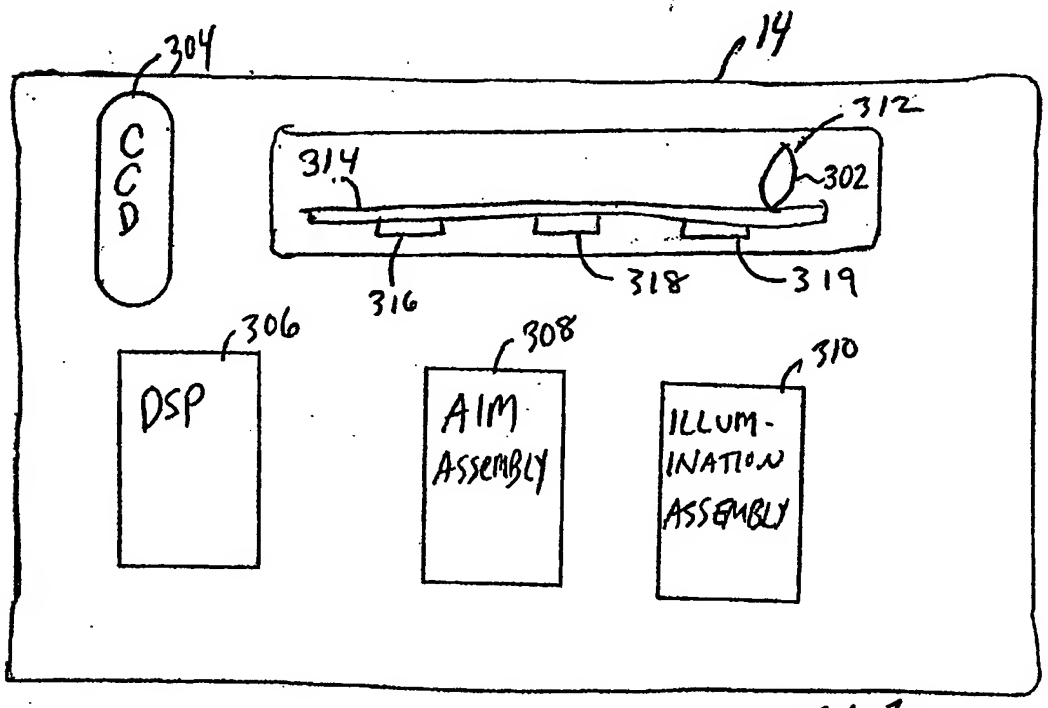
304
14
312
CCD
314
302
316
318
319
306
308
310
DSP
AIM Assembly
Illum-ination Assembly

FIG. 3

| Pin Number | Signal Name | I/O | Comments |
|---|---|---|---|
| 1 | GND | PWR | Ground |
| 2 | PCLK | O | Pixel Clock |
| 3 | GND | PWR | Ground |
| 4 | HREF | O | Horizontal Pixel Valid Clock (Sync) |
| 5 | VCC_MOTOR | PWR | Focus Control Motor Power |
| 6 | VCC_ILLUM | PWR | IlluminationPower |
| 7 | REG_RESET* | I/O | I2C Register Reset |
| 8 | VCC | PWR | CCD/Aiming Power |
| 9 | VCC | PWR | CCD/Aiming Power |
| 10 | EXSFT | I | External Frame Sync. |
| 11 | ILLUM_ENB* | I | Illumination Enable |
| 12 | AIM_ENB* | I | Aim Enable |
| 13 | PIX_D0 | O | Pixel Data Bit 0 |
| 14 | PIX_D1 | O | Pixel Data Bit 1 |
| 15 | PIX_D2 | O | Pixel Data Bit 2 |
| 16 | PIX_D3 | O | Pixel Data Bit 3 |
| 17 | PIX_D4 | O | Pixel Data Bit 4 |
| 18 | PIX_D5 | O | Pixel Data Bit 5 |
| 19 | PIX_D6 | O | Pixel Data Bit 6 |
| 20 | PIX_D7 | O | Pixel Data Bit 7 |
| 21 | FOCUS_CTRL1 | I | Focus Control Line 1 |
| 22 | VREF | O | Vertical Frame Valid Clock (Sync) |
| 23 | EXHT | I | External Horizontal Clock |
| 24 | I2C_SDA | I/O | I2C Data |
| 25 | I2C_SCL | I | I2C Clock |
| 26 | GND | PWR | Ground |
| 27 | MCKI | I | Master Clock |
| 28 | GND | PWR | Ground |
| 29 | FOCUS_CTRL2 | I | Focus Control Line 2 |
| 30 | CS* | I | Chip Select |
| 31 | FRAME_SHIFT | O | Frame shift after exposure for Mode 1 |

FIG. 4

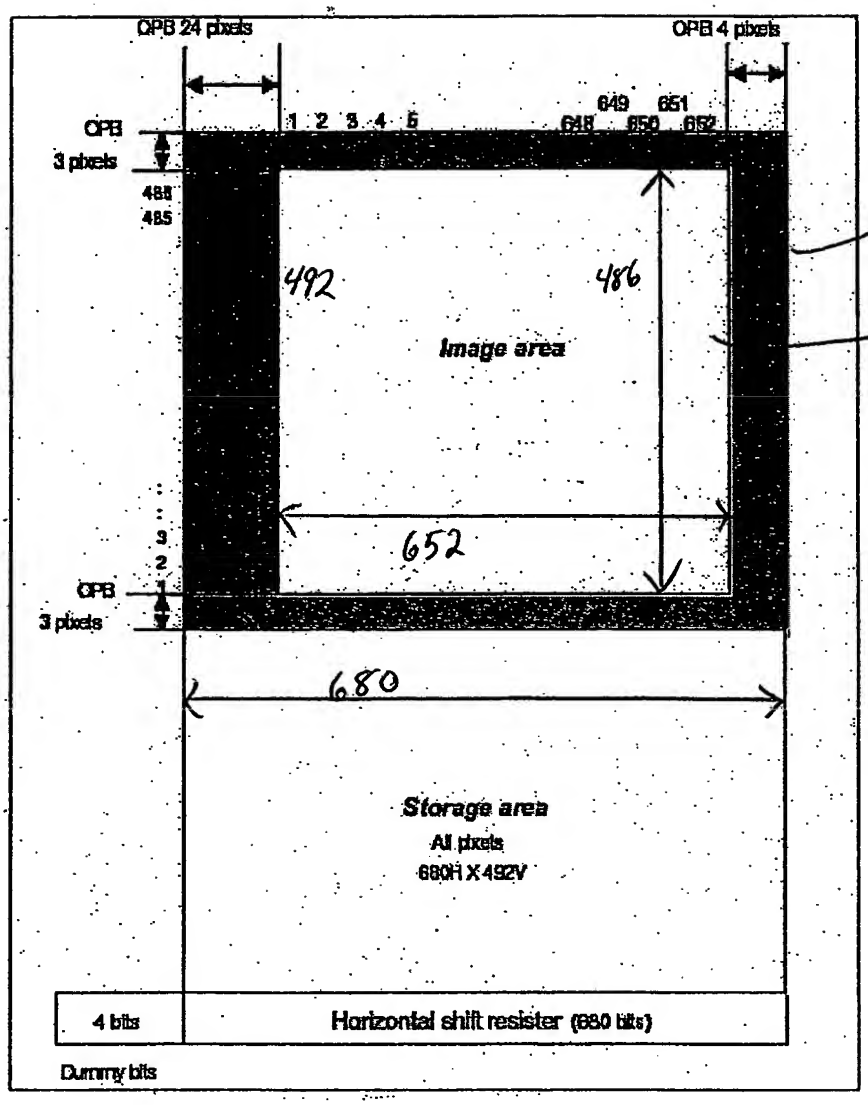
OPB 24 pixels
OPB 4 pixels
1 2 3 4 5
649 651
648 650 652
OPB
3 pixels
488
485
492
486
Image area
502
504
652
3
2
1
OPB
3 pixels
680
Storage area
All pixels
680H X 492V
4 bits
Horizontal shift resister (680 bits)
Dummy bits
500

FIG. 5

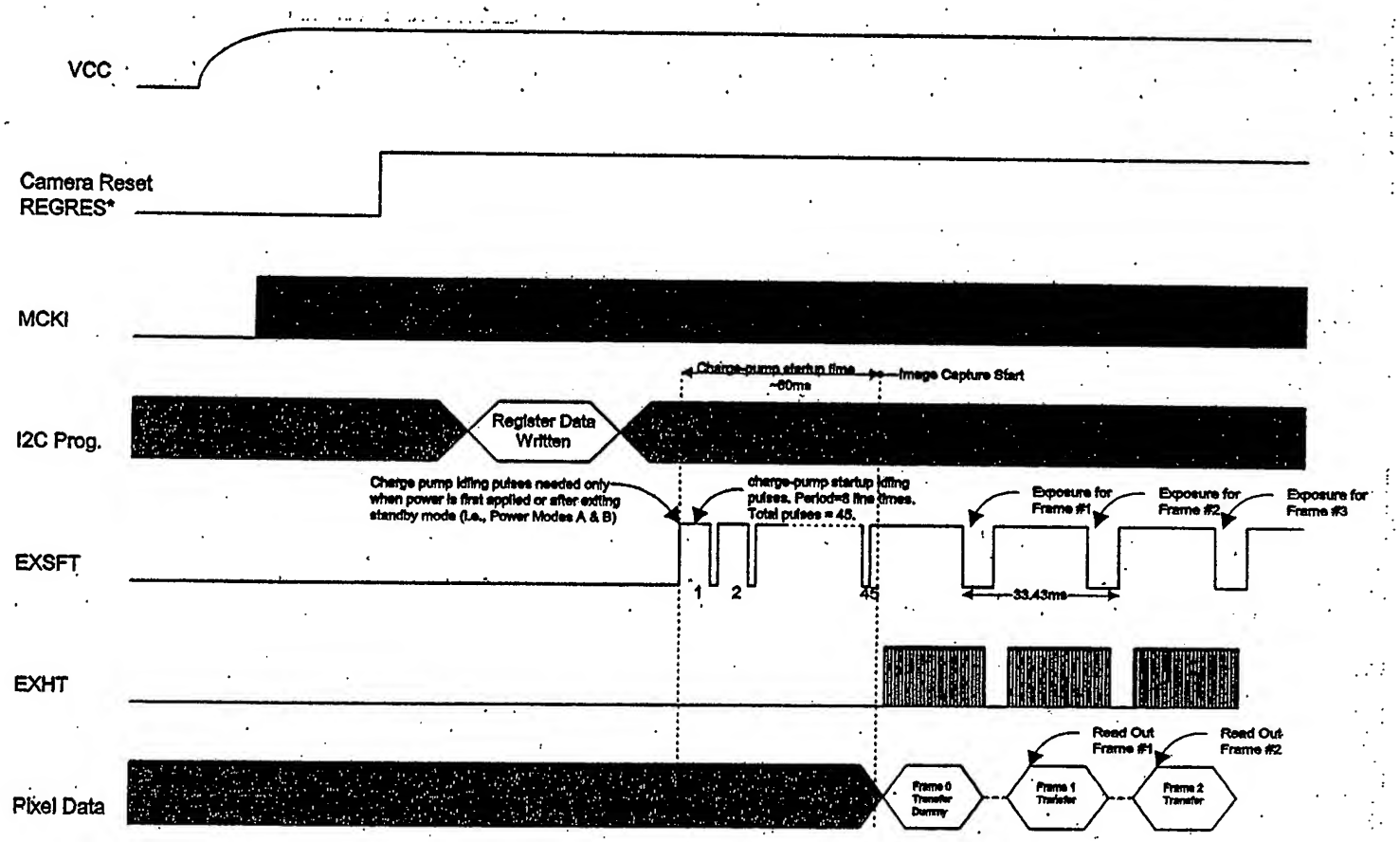
VCC
Camera Reset
REGRES*
MCKI
Charge-pump startup time ~60ms
Image Capture Start
I2C Prog.
Register Data Written
Charge pump idling pulses needed only when power is first applied or after exiting standby mode (i.e., Power Modes A & B)
charge-pump startup idling pulses. Period=8 line times. Total pulses = 45.
Exposure for Frame #1
Exposure for Frame #2
Exposure for Frame #3
EXSFT
1
2
45
33.43ms
EXHT
Read Out Frame #1
Read Out Frame #2
Pixel Data
Frame 0 Transfer Dummy
Frame 1 Transfer
Frame 2 Transfer

FIG. 6

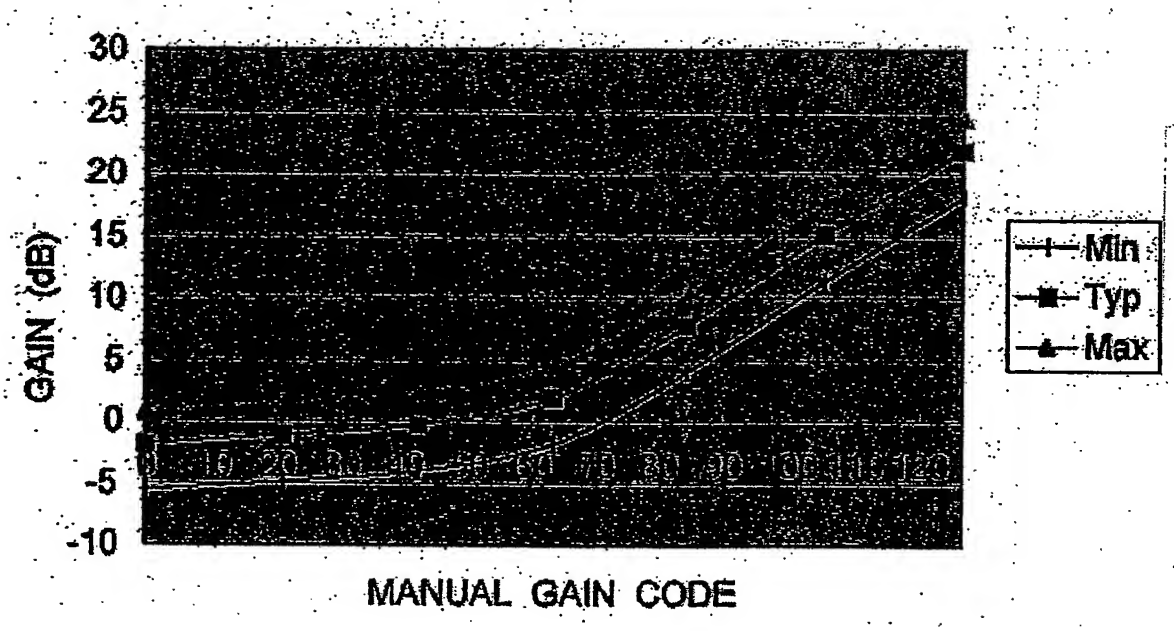


FIG. 7

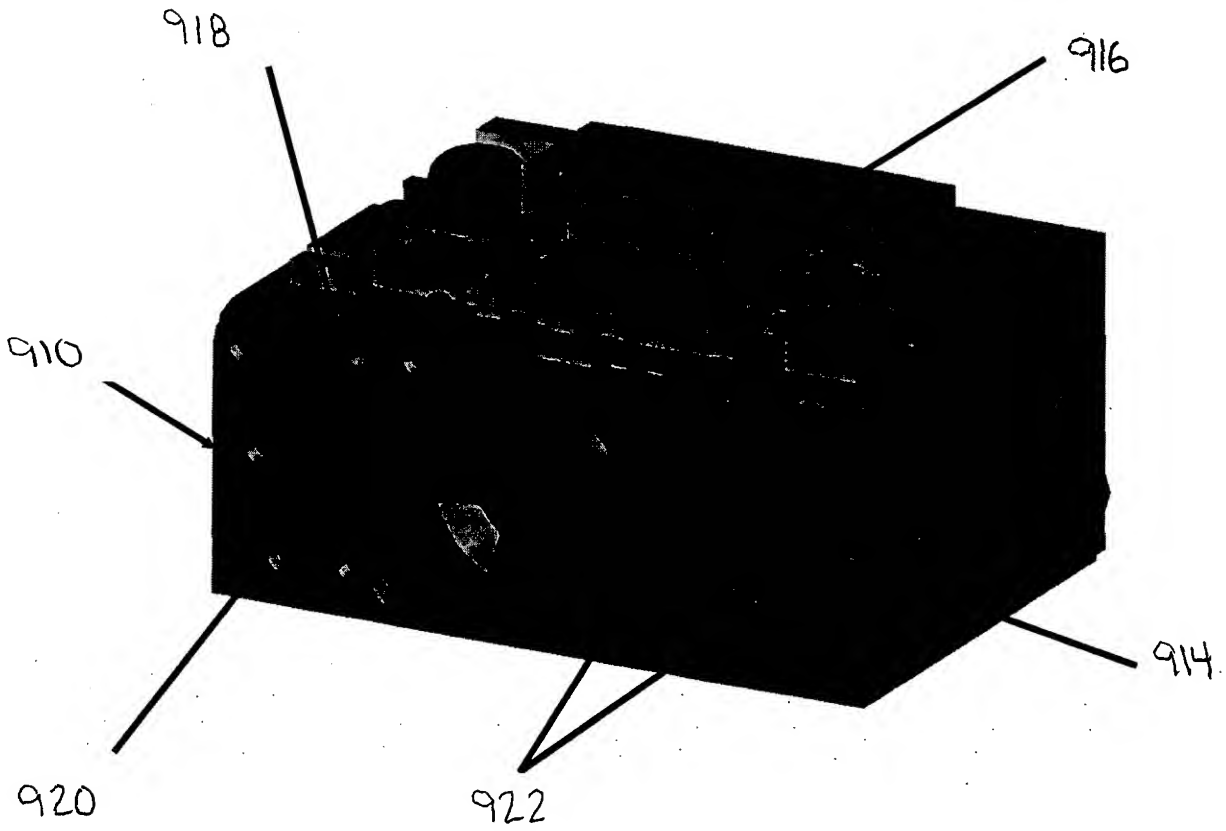


FIG. 8

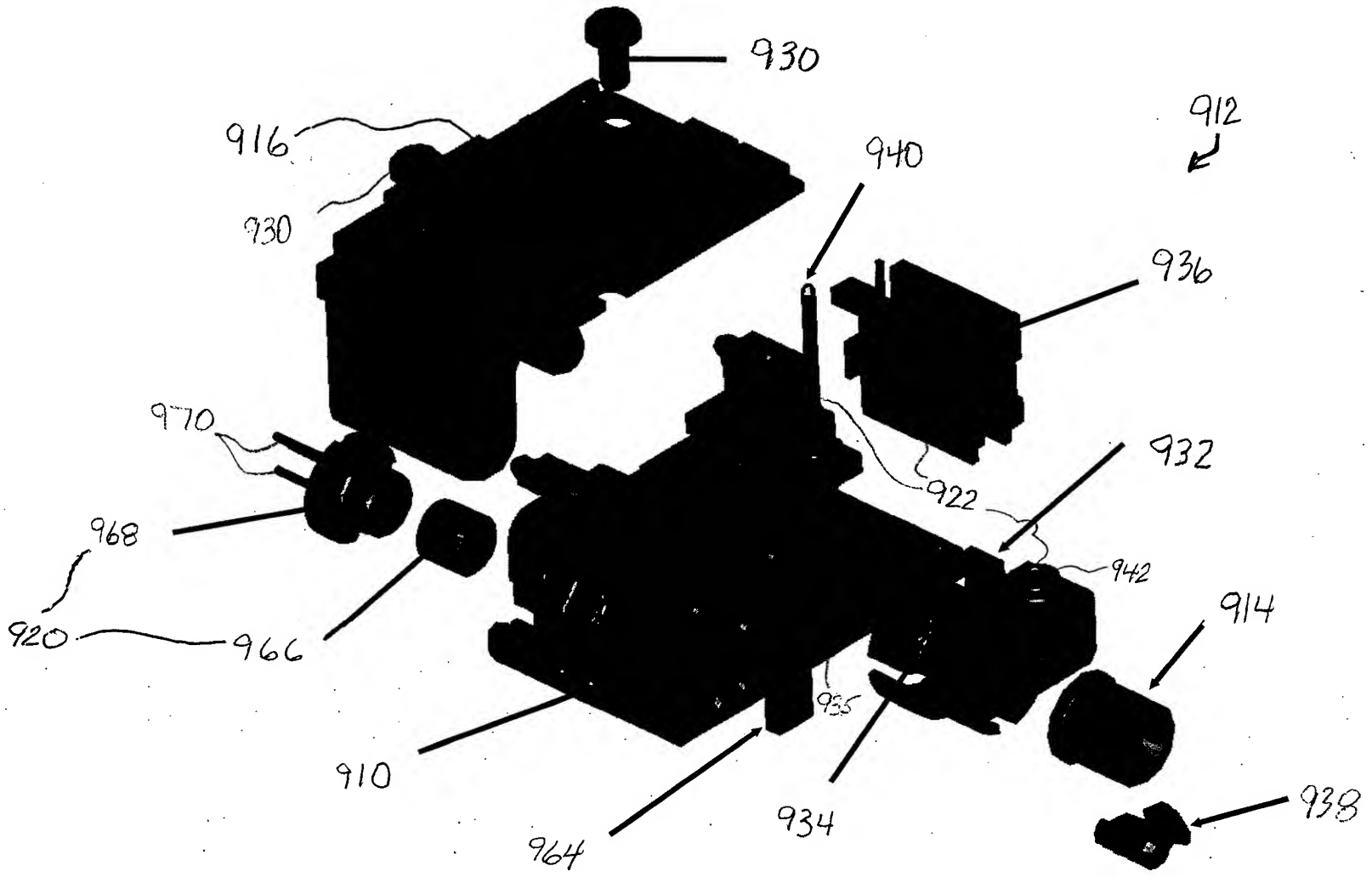
930
916
930
912
940
936
970
922
932
968
942
920
966
914
935
910
934
964
938

FIG. 9

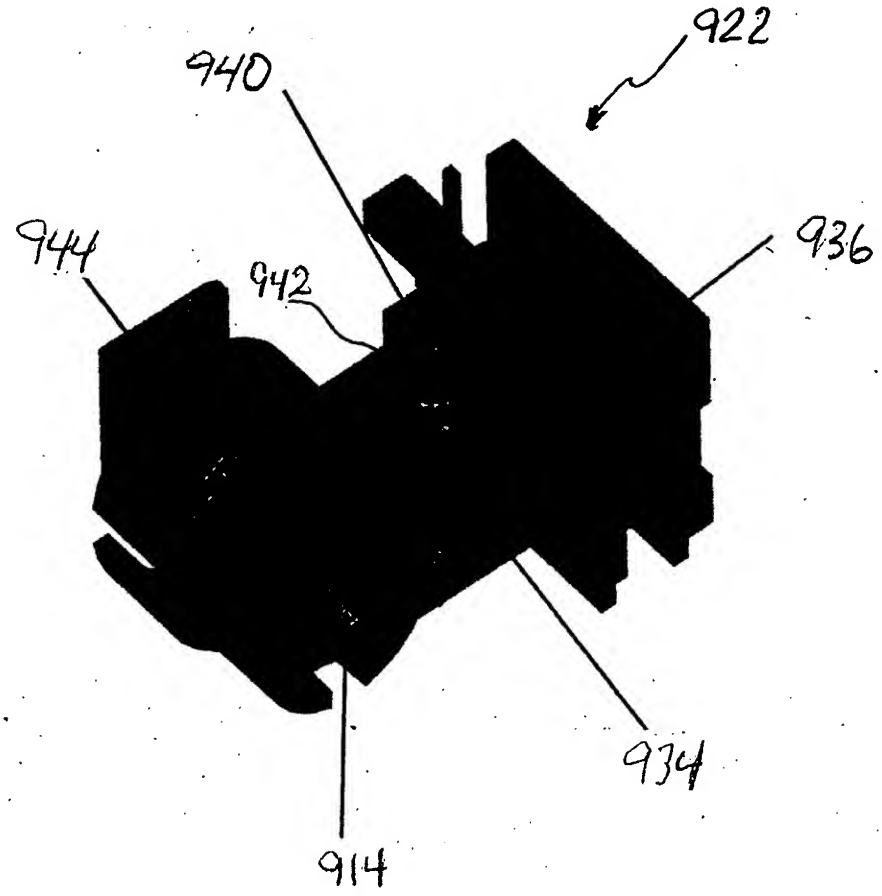


FIG. 10

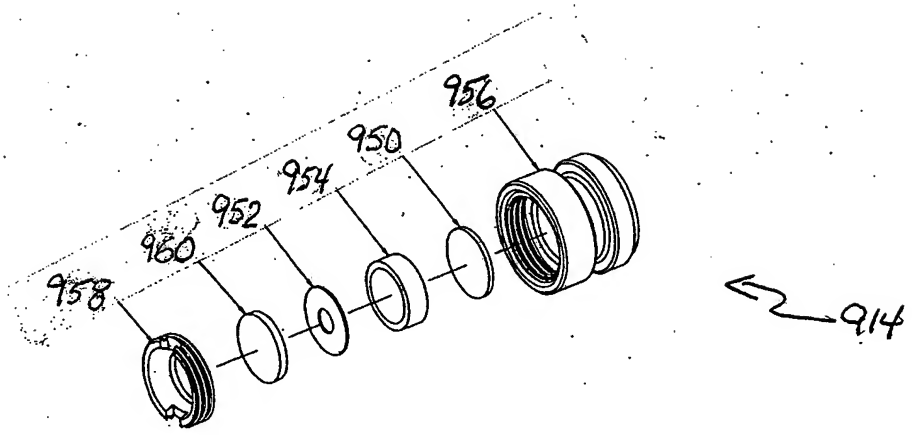


FIG. 11